**Register Module:**

* The Acknowledgment bit going to AXI module is a one clock cycle **pulse** that can start when read enable is set to ‘1’.
* Whenever data changes in a register it sends a pulse to top entity signaling change.

**SPI Module:**

* There shall be an Ack in port for the register module. SPI module will only update its settings based on what is coming from the register module after it sees a pulse on the Ack port.
* SPI\_CLK and AXI\_CLK are assumed to be synchronized with each other during slave operation.

**Top Entity:**

**FIFOs:**

* Depth is set at 16, width = C\_NUM\_TRANSFER\_BITS